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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/630,684	07/31/2003	Magdy Salama	2929-0223P	7661
7590	09/22/2004		EXAMINER	
Larry J. Palguta Honeywee Law Department 3520 Westmoor Street South Bend, IN 46628			LAXTON, GARY L	
			ART UNIT	PAPER NUMBER
				2838

DATE MAILED: 09/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/630,684	SALAMA ET AL.	
	Examiner	Art Unit	
	Gary L. Laxton	2838	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on _____.
- 2a) This action is **FINAL**. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-28 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1-28 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 17 November 2003 is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date. _____ .
3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date <u>09/05/03</u> .	5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)
	6) <input type="checkbox"/> Other: _____.

DETAILED ACTION

Inventorship

1. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Specification

2. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claim 17 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 17 recites “capacitors arranged in a zigzag pattern”; it is unclear what the applicant means by arranging in a zigzag pattern. What does the applicant consider a zigzag pattern to be? There is no definition of zigzag in the claim. Resultantly, the phrase is given no patentable weight.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-12 and rejected under 35 U.S.C. 103(a) as being unpatentable over Gak et al Gallios et al.

Claims 1 and 18; Gak et al discloses a high-voltage power supply and method, comprising: a power scaling section (11) receiving an input voltage signal (Vin) and converting the input voltage signal to a controllable DC voltage; a push-pull converter (13, 14A, 14B) for converting the controllable DC voltage to a high-frequency wave.

However, Gak et al do not disclose a voltage multiplier receiving the high-frequency wave generated by the push-pull converter and performing successive voltage doubling operations to generate a high-voltage DC output.

Gallios et al teaches a two stage full-wave Cockroff-Walton high voltage multiplier 20 for receiving high frequency wave generated by a push pull converter for performing successive voltage doubling operations to generate a high voltage dc output in order to provide high output voltage to a load requiring very high output voltage.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Gak et al to include a voltage multiplier for receiving high frequency wave generated by a push pull converter for performing successive voltage doubling operations to generate a high voltage dc output in order to provide high output voltage to a load requiring very high output voltage as taught by Gallios et al.

Claims 2 and 19; Gak et al further disclose: a control module (19) for controlling the power scaling section and the push-pull converter.

Claims 3 and 20; Gak et al further disclose wherein the power scaling section includes a switching element (12), a duty cycle of which controls the amplitude of the controllable DC voltage, and the control module outputs a gate switching signal (20) to the switching element (12) of the power scaling section (11) as a function of a desired output voltage of the high-voltage power supply.

Claims 4 and 21; Gak et al further disclose wherein the control module receives a feedback signal (16) based on the output of the power scaling section to adjust the gate switching signal (20).

Claims 5 and 22; Gak et al further disclose wherein the push-pull converter includes a plurality of switching elements (14A, 14B) and a transformer (15) for generating the high-frequency wave, and the control module outputs gate switching signals (CLK-PPA, CLK-PPB)

to the switching elements (14A, 14B) of the push-pull converter (13) to control the frequency of the high-frequency wave.

Claims 6 and 23; Gak et al further disclose the switching elements are MOSFET switching elements.

Claims 7 and 24; Gak et al further disclose the high-frequency wave is a square wave.

Claims 8 and 25; Gallios et al disclose wherein the frequency of said high-frequency wave is approximately 100 kHz (col. 5 line 31).

Claims 9 and 26; Gak et al further disclose the controllable DC voltage is in the range of approximately 0-to 28 kV.

Claims 10 and 27; Gak et al further disclose in the power supply generates an output voltage of in the range of approximately 0-to-30 kV, DC.

Claims 11 and 28; Gak et al further disclose in the high-frequency wave has an amplitude of approximately 0-to-1 kV.

Claim 12; Gak et al further disclose wherein the control module is an analog controller.

7. Claims 13-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gak et al (US 6,141,225) and Gallios et al (US 4,893,227) in view of Adasko et al (US 5,414,224).

Claims 13-17; Gak et al and Gallios et al disclose the claimed subject matter in regards to claim 1 supra, except for the voltage multiplier includes voltage doubler stages on a circuit board and the high-voltage power supply further comprises an insulation system associated with the circuit board. And, the insulation system is a multi-layer system of n layers of insulation and m

conducting strips positioned between successive insulating layers; wherein the insulation system is a field-controlled multi-layer insulation system. And lastly, the plurality of voltage doubler stages are divided among multiple circuit boards, separate from the power scaling section and the push-pull converter.

First, it has been held that forming in one piece an article which has formerly been formed in two pieces and put together (such as integrating circuit components on a circuit board) involves only routine skill in the art. *Howard v. Detroit Stove works*, 150 U.S. 164 (1893). Therefore, integrating parts on a circuit board is routinely obvious to one having ordinary skill in the art.

Secondly, duplication of parts is well known in the art; since it has bee held that mere duplication of the essential working parts of a device (such as connecting plural circuit boards together) involves only routine skill in the art. *St. Regis Paper Co. v. Bemis Co.*, 193 USPQ 8. Therefore, duplicating multiple voltage doubler circuit boards is routinely obvious to one having ordinary skill in the art.

Adasko et al teach forming a multilayered printed circuit board having layers with insulation between; and conducting strips between as well.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Gak et al and Gallios et al to include the voltage multiplier on a circuit board and further comprising an insulation system associated with the circuit board comprising insulating layers and conducting strips to form a field-controlled multi-layer insulation system in order to form an integrated small form multilayered printed circuit board for use in an electronic power supply circuit. And further, it would have been obvious to one having

ordinary skill in the art at the time the invention was made to modify Gak et al and Gallios et al to include plural circuit boards separate from separate from the power scaling section and the push-pull converter in order to provide a plurality of separate voltage circuits to provide high voltage power to a plurality of different loads, since duplicating parts is routine to those skilled in the art.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. US 5,289,360 Canova disclose a DC/DC converter with a voltage multiplier rectifier connected at the output; US 5,138,249 Capel discloses a push pull converter with a power scaling circuit connected upstream; US 3,819,942 Hastwell et al disclose a push pull converter with a voltage doubler connected at the output.

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9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gary L. Laxton whose telephone number is (571) 272-2079. The examiner can normally be reached on Monday thru Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Sherry can be reached on (571) 272-2084. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Gary L. Laxton
Patent Examiner
Art Unit 2838

